

**Application Note - 001b**

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**STABLE PRELOAD PROVIDES  
WIDE RANGE TRIMMING TO DC-DC CONVERTER**

By

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### INTRODUCTION

VICOR's second-generation DC-DC converters are programmable from 10% to 110% of their nominal output voltage ( $V_{nom}$ ). However, this often requires a minimum load, when the output voltage is programmed below 75% of  $V_{nom}$ , and is always required below 25% of  $V_{nom}$ . An active preload, instead of a fixed resistor, avoids unnecessary power losses.

Figure 2 describes a circuit for use with any VICOR second-generation DC-DC converter. The circuit makes use of a 48/28 volts (input/output) module (VICOR's DC-DC converter module V48B28C250A) to illustrate the design approach through calculations of circuit components' values.

### GENERAL CIRCUIT DESCRIPTION

The voltage control section of the circuit allows linear setting of the module's output voltage, between 2.8 V and 30.8 V (10% and 110% of its nominal output voltage ( $V_{nom}$ )). The preload section of the circuit does not compare the module's output voltage against the module's programmed output voltage (e.g., in order to determine as to whether it should or not load the module), it simply loads the circuit at a preset level, as a function of +Out, whether the module requires loading or not, thereby providing a circuit which is inherently stable.

### VOLTAGE CONTROL SECTION

#### **R<sub>2</sub>, R<sub>v1</sub>, R<sub>3</sub>**

The module's internal reference voltage is 1.23 V, which, compared to the input voltage at terminal SC, determines the module's output voltage (see VICOR's data sheet for more information on its modules' internal reference voltages). R<sub>2</sub>, R<sub>v1</sub>, and R<sub>3</sub> are selected to provide 1.23 V (- 90% +10%) at the module's SC terminal, thereby enabling users to set the module's output voltage between 10% and 110% of its nominal voltage output ( $V_{nom}$ ).

### PRELOAD SECTION

Two points of operation are selected (P<sub>3</sub> and P<sub>4</sub>). They set the voltage and current levels at which the circuit will apply a load across the output terminals of the module. Curve "a" (Figure 1) represents the typical minimum load current required for a V48B28C250A module to function at voltages lower than 57.1% of its nominal voltage output ( $V_{nom}$ ).

For the V48B28C250A module, the equation of curve "b" that passes through points P<sub>1</sub> and P<sub>2</sub> is:

$$y = mx + b$$

Where:  $m = -24.26$   
 $b = 18.015$

The slope of curve “b”, for the V48B28C250A module, is representative of the slope of V48B28C250A modules, which may require preloads at higher output voltages (e.g., 75% of  $V_{nom}$ ). VICOR specifies 75% of its modules’ nominal output voltage as the worst-case voltage level at which a preload may be required. If we set one point of operation ( $P_3$ ) at 80% of  $V_{nom}$ , we are well within the guaranteed area of operation should the module require loading at the 75% output voltage level. For the other point of operation ( $P_4$ ), if we keep the same slope for curve “c” as for curve “b”, and shift it so it will pass through  $P_3$  (80% of  $V_{nom}$ ), we obtain:

$$P_4 = 808 \text{ mA}$$

### **R<sub>10</sub>**

In order to reduce power dissipation for  $Q_1$  to a minimum, let us set the value of  $R_{10}$  so that it sustains the maximum circuit load (distributed between  $R_{10}$  and  $Q_1$ ) at 10% of  $V_{nom}$  (2.8 V);

$$\begin{aligned} V_4 &= 2.8 \text{ V} - V_{sat-Q1} \\ V_4 &= 2.0 \text{ V} \\ R_{10} &= V_4/808 \text{ mA} \\ R_{10} &= 2.47 \text{ ohms, } R_{10} = 2.4 \text{ ohms (nearest standard value)} \end{aligned}$$

Where;  $V_{sat-Q1} = 0.8 \text{ V}$

### **R<sub>4</sub>, R<sub>5</sub>**

$R_5$ ’s ohmic value is set such that the input voltage to the Op-Amp never exceeds the Op-Amp’s rail supply. Selecting a maximum arbitrary input voltage of 4.0 V at 110% of  $V_{nom}$  yields  $R_5 = 1.5\text{K}$  ohms (nearest standard value), for  $R_4 = 10\text{K}$  ohms.

### **R<sub>F</sub>, R<sub>1</sub>, R<sub>6</sub>, R<sub>7</sub>**

We want the preload  $R_{10}$  to begin drawing current at 80% of  $V_{nom}$  ( $P_3$ ). Therefore,  $V_3$  must be equal to zero at that point, and must begin to rise as  $V_{nom}$  falls further towards 10% of  $V_{nom}$ , at which latter point ( $P_4$ ) it must equal 2.8 V, which voltage will be compared to  $V_4$ , which must equal 2.0 V at that same point. In order to obtain these voltages and resistors’ values, we only need solve a linear algebraic equation for two unknowns;

We know that, at point  $P_3$ ,  $V_1 = 2.922 \text{ V}$ , and at point  $P_4$ ,  $V_1 = 0.365 \text{ V}$ ;  
 $IC_{3/4}$  is a differential summing amplifier configuration (hence, the negative factor for the  $x$  term).

Therefore:

$$-2.922x + y = 0 \text{ V} \tag{1}$$

$$-0.365x + y = 2.0 \text{ V} \tag{2}$$

Where;  $x$  = The Op-Amp’s gain for its inverting input, or;  
 $x = (R_F/R_1)$   
 $y = V_2$  multiplied by the Op-Amp’s gain for its non-inverting input, or;  
 $y = V_2 (1 + R_F/R_1)$

Equations (1) and (2) yield:

$$\begin{aligned} x &= 0.782 \text{ A}_v \\ y &= 2.285 \text{ V} \cdot \text{A}_{v+} \end{aligned}$$

Where;  $A_{v+}$  = Voltage gain of the Op-Amp for the non-inverting input  
 $A_{v-}$  = Voltage gain of the Op-Amp for the inverting input  
 $V$  = Voltage at the Op-Amp's input (inverting or non-inverting).

For the inverting input:  $A_{v+} = R_F/R_1$ ; If we let  $R_F = 10K$ , then  $R_1 = 12,778$  ohms,  $R_1 = 13K$  (nearest standard value).

For the non-inverting input: Substituting known values in  $y = V_2(1 + R_F/R_1)$ , and rearranging, we obtain:

$$V_2 = 2.285 / (1 + 10K/13K)$$
$$V_2 = 1.29 \text{ V}$$

If we set  $R_7 = 1.5K$ , then  $R_6 = 4.31K$ ,  $R_6 = 4.3K$  (nearest standard value).

### **R<sub>9</sub>, R<sub>11</sub>**

These two resistors are current limiting (20 mA) for the LM124 Quad Op-Amp.

### **C<sub>1</sub>, C<sub>2</sub>**

$C_1$  is a decoupling capacitor.  $C_2$  provides a -3dB breakpoint at 159 Hz (-6dB/octave roll-off).

## **CONDUCTOR ROUTING**

The output of  $IC_{1/4}$  should be tied as close as is feasible to the SC terminal, due to the high input impedance of the module's internal Op-Amp.

All points common to the zero of the split-supply should be connected through a common plane, or a star topology, as close to the -S terminal as is feasible.

$R_8$  and  $R_{10}$  should be tied together on the -Out rail to avoid ground loops. Tying these two resistors together at the same point provides common mode rejection of signals, which may develop between their common point of connection on the -Out rail and the zero of their split-supply, tied to the -S rail.

Absolutely NO current may flow from the -Out or +Out terminals to a load, going through the -S or +S terminals.

## **PARTS LIST**

$R_1$ through $R_9$ , and $R_{11}$	: 1/4 watt, 5%
$R_{10}$	: 2 watts, 5%
$C_1$ and $C_2$	: 0.1 uF ceramic
$IC_{1-4}$	: LM104 (low cost Quad Op-Amp)
$Q_1$	: TIP112 (low cost Darlington, TO-220 case)
Heat sink	: 24.4 °C/W (TIP112; $P_{D-Q1} = 4$ watts, $T_a = 40$ °C)

### Typical Performance of V48B28C250A

$V_{out}$ (V)	$R_{trim}$ ( $\Omega$ )	$I_L$ (mA)
20.006	2K51	0
18.015	1K8	0
15.997	1K31	17
14.02	990	34
11.983	740	58
9.995	550	92
8.042	400	135
5.981	270	213
4.095	170	355
2.634	100	634

Table 1 - Preload Requirements

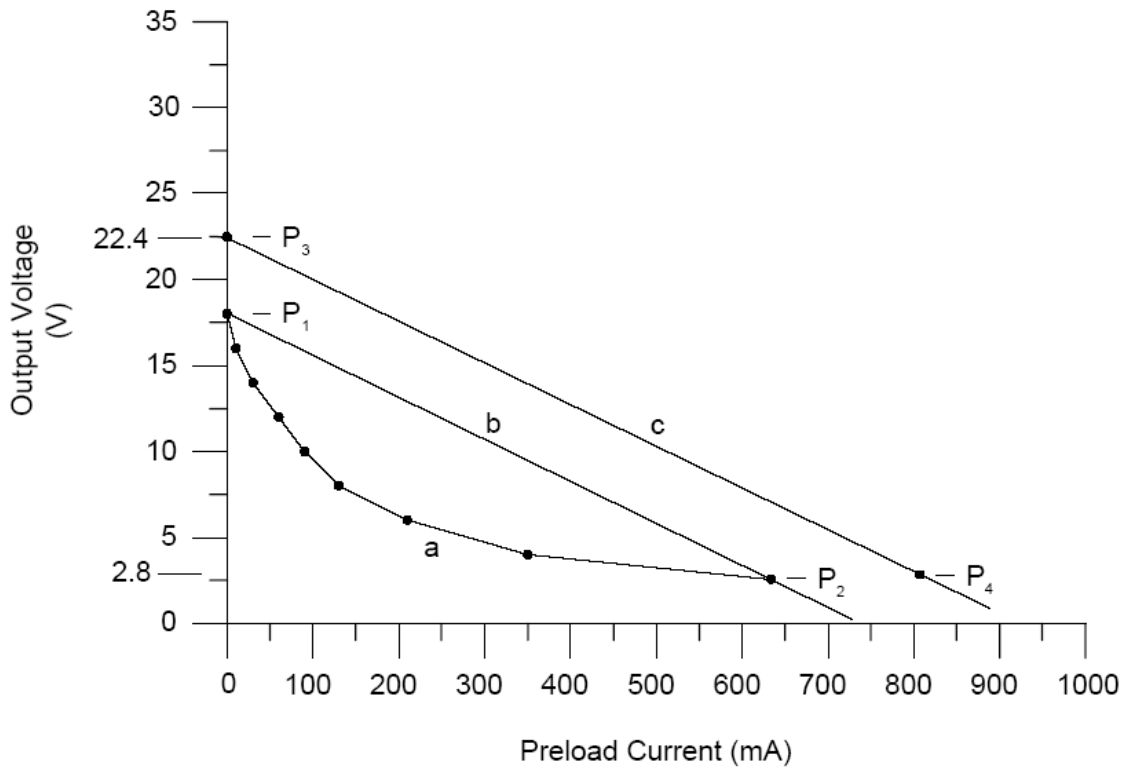


Figure 1

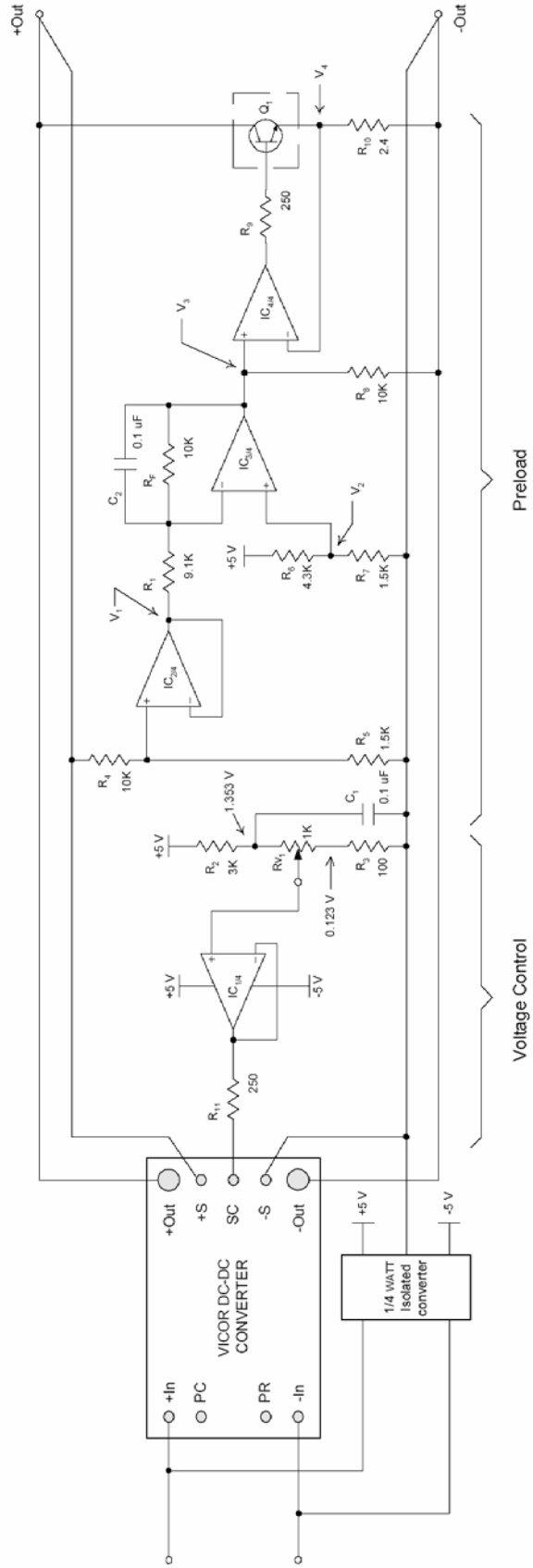


Figure 2